SEMICONDUCTOR MEMORY DEVICE, ELECTRONIC CARD

AND ELECTRONIC DEVICE

CROSS REFERENCE TO RELATED APPLICATIONS

5   This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2002-207383, filed on July 16, 2002; the entire contents of which are incorporated herein by reference.

10   BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor memory device, and more particularly to an electrically erasable programmable non-volatile semiconductor memory

15 (EEPROM) having bit line selection transistors arranged at a cell array end.

Description of the Related Art

In a mass NAND-type EEPROM configuration, bit lines arranged at a fine pitch are divided into odd and even ones,

20 and either one of them is selectively connected to a sense amp. In this case, bit line selection transistors are arranged in a cell array at bit line ends to select odd and even bit lines.

Fig. 13 shows a configuration covering from a cell

25 array 1 to a sense amp 2 in such the NAND type EEPROM, focusing attention on odd bit lines BLo (BLo0<k> - BLo7<k>) and adjacent even bit lines BLe (BLe0<k> - BLe7<k>). There

is an arrangement region 3 for bit line selection transistors Q0-Q15 between the c 11 array 1 and the sense amp 2. The cell array 1 comprises NAND cell units U arrayed. Each unit includes plural (16 in the shown

5   example) non-volatile memory cells MC0-MC15 serially connected. Each NAND cell unit U has one end connected to the bit line BLo or BLe via a selection transistor S1 and the other end connected to a common source line CELSRC via a selection transistor S2.

10   The memory cells MC0-MC15 have control gates respectively connected to word lines WL0-WL15, which are arranged to intersect the bit lines BLo and BLe. The selection transistors S1 and S2 have gates connected to selection gate lines SGD and SGS, which are arranged in

15   parallel with the word lines. The ends of the bit lines BLo and BLe in the cell array are connected, via the bit line selection transistors controllable by selection signals BLSo and BLSe, to common sensing bit lines SBL, which are connected to the sense amp 2. For example, the

20   bit lines BLo0<k> and BLe0<k> are connected via the bit line selection transistors Q0 and Q1 to the common sensing bit line SBL0<k>.

        The bit line selection transistors Q0-Q15 are required to consist of a high voltage transistor because a

25   high erasing voltage is applied to the bit line during data erase. This situation is specifically described. When data is written in the NAND-type EEPROM, the p-type well is

hold at 0V and a write voltage of approximately 20V is applied to the selected word line to inj ct electrons from the channel region into the floating gate of the selected memory cell. This results in a higher threshold of the

5 memory cell in a written state (for example, the state of "0" data). On the other hand, data is erased in a block batch of cells sharing the p-type well. During data erase, while all word lines in the cell block are held at 0V and the bit lines are floated, an erase voltage of

10 approximately 20V is applied to the p-type well to discharge the charges from inside the floating gate of the memory cell to the substrate. This results in a lower threshold of the memory cell in an erased state.

During data erase, the n-type diffusion layer

15 connected to the bit line is forward biased relative to the p-type well. Therefore, the erase voltage of 20V may appear even on the floating bit line. The bit line selection transistors are formed in another p-type well different from the p-type well in the cell array 1, and are

20 isolated from the p-type well in the cell array 1. When the voltage on the bit line is elevated up to 20V, however, a junction breakdown may possibly arise between the n-type source/drain diffusion layer of the bit line selection transistor and the p-type well, resulting in destruction of

25 peripheral circuits. For the purpose of protection of the peripheral circuits, the bit line selection transistor should consist of a high voltage transistor.

As described above, the need for the high-voltage bit
lin selection transistors may add constrains to downsize
them. Ther fore, when the bit lines are arranged at a much
finer pitch in the cell array 1, the layout of bit line
5   selection transistors causes a problem.

SUMMARY OF THE INVENTION

The present invention has been made in consideration
of such the situation and accordingly has an object to
10   provide a semiconductor memory device capable of arranging
bit line selection transistors without reduction of the
area efficiency. An electronic card including the memory
device mounted thereon is also provided, as well as an
electronic device utilizing the electronic card.

15   An aspect of the semiconductor memory device
according to the present invention comprises a cell array
including bit lines arranged at a uniform pitch; and a
plurality of bit line selection transistors connected to
respective bit line ends for selectively connecting the bit
20   line to a sense amp. The bit line selection transistors
are translationally arrayed in a direction perpendicular to
the bit line at an average array pitch greater than eight
times the pitch of the bit lines.

Another aspect of the semiconductor memory device
25   according to the present invention comprises a cell array
including bit lines arranged at a uniform pitch; and a
plurality of bit line selection transistors connected to

respective bit line ends for selectively connecting the bit line to a sense amp. The bit line selection transistors are translationally arrayed in a direction perpendicular to the bit line at an average array pitch deviated from an

5 integer multiple of the pitch of the bit lines.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more fully understood from the following detailed description with reference to

10 the accompanying drawings, in which:

Fig. 1 shows a layout of bit line selection transistors according to an embodiment of the present invention;

Fig. 2 shows a layout of bit line selection

15 transistors according to another embodiment;

Fig. 3 shows a transistor block B0 in Fig. 2 and its wiring layout;

Fig. 4 shows a transistor block B1 in Fig. 2 and its wiring layout;

20 Fig. 5 shows a transistor block B2 in Fig. 2 and its wiring layout;

Fig. 6 shows a transistor block B3 in Fig. 2 and its wiring layout;

Fig. 7 shows a transistor block B4 in Fig. 2 and its

25 wiring layout;

Fig. 8 shows a layout of bit line selection transistors according to another embodiment;

Fig. 9 shows a layout of bit line selection transistors according to another embodiment;

Fig. 10 shows another embodiment applied to a digital still camera;

5   Fig. 11 shows the internal configuration of the digital still camera;

Figs. 12A to 12J show other electronic devices to which the embodiment is applied;

Fig. 13 shows a cell array arrangement in a NAND-type

10   EEPROM in the art; and

Fig. 14 shows a layout of bit line selection transistors in a NAND-type EEPROM of a comparative example.

DETAILED DESCRIPTION OF THE EMBODIMENTS

15   A NAND-type EEPROM according to an embodiment of the present invention will be described below with reference to the drawings. This EEPROM includes a cell array similar to the cell array 1 in Fig. 13. As shown in Fig. 13, the cell array 1 has a matrix arrangement that includes plural (16

20   in the shown example) non-volatile memory cells MC0-MC15 serially connected to form a NAND cell unit U, each pair of adjacent cells sharing a common source/drain diffusion layer. Each NAND cell unit U has one end connected to the bit line BLo or BLe via the selection transistor S1 and the

25   other end connected to the common source line CELSRC via the selection transistor S2. The memory cells MC0-MC15 have respective control gates connected to the word lines

WL0-WL15 that are arranged to intersect the bit lines BLo, BLe. Th selection transistor S1, S2 have respective gates connected to the selection gate lines SGD, SGS that are arranged in parallel with the word lines.

5   To facilitate understanding of the layout of bit line selection transistors according to the embodiment of the invention, a comparative example is described first. Fig. 14 shows an arrangement region 3 for the bit line selection transistors when data input/output is executed on an 8 bit

10   basis at a certain column address <k>. Specifically, it is an exemplary layout showing a total of 16 bit lines including 8 odd and 8 even bit lines, BLo0<k>, BLe0<k>, ..., BLo7<k>, BLe7<k>; and the corresponding 16 bit line selection transistors Q1-Q15. As shown, the bit line

15   selection transistors are arranged in 2 rows of 8 stages in the bit line direction, each pair of adjacent transistors corresponding to odd and even bit lines, sharing a source/drain diffusion layer. In other words, 8 transistors are arranged in the bit line direction and 2 in

20   a direction intersecting thereto. The bit line selection transistors have gates (hatched) that are continuously patterned in the direction intersecting the bit line for receiving the selection signals BLSo, BLSe.

        The bit line selection transistors on 8 stages are

25   arranged at a pitch corresponding to 8 bit lines, b (= 8a), where a defines a bit line pitch. For each pair of transistors sharing a common diffusion layer, the common

diffusion layer is connected to the respective one of sensing bit lines SBL0 - SBL7. From the bit line selection transistors in 8 stages × 2 rows, 8 sensing bit lines SBL0<k> - SBL7<k> are led out and connected to 8 sense amps

5   S/A0 - S/A7. These 8 sense amps S/A0 - S/A7 provide 8 bit data, which is input/output via I/O buffers simultaneously at one column address.

In the layout of Fig. 14, if the bit line pitch a is further finely patterned, the array pitch of the bit line

10 selection transistors, b - 8a, hardly isolates the bit line selection transistors from one another reliably. To the contrary, it can be considered that the bit line selection transistors may have an array pitch of b - 16a corresponding to 16 bit lines. In this case, the bit line

15 selection transistors are arranged in one row of 16 stages for 16 bit lines. This arrangement results in a longer period, however, than that required for arrangement of the bit line selection transistors and extremely lowers the chip area efficient.

20   On the other hand, Fig. 1 shows a layout of bit line selection transistors in the NAND-type EEPROM according to the embodiment. As shown in the comparative example, the odd and even bit lines BLo, BLe in the cell array are arrayed at the pitch a, and the bit line selection

25 transistors are arranged at the bit line ends in 2 rows of 8 stages for 16 bit lines. To the contrary, Fig. 1 shows an exemplary arrangement of 20 bit lines (20BLs) in 10

stages × 2 rows. The total number of bit lines is generally equal to an integer multiple of 16, or 16n. As is in the embodiment, if the total number of bit lines is equal to 80n, the bit line selection transistors may be

5 arranged in 10 stages × 8 rows for every 80 bit lines (20BLs × 4) as shown. The arrangement in n stages × m rows (n, m are integers of 2 or more), such as 10 stages × 8 rows, is called a translation arrangement.

This arrangement of the bit line selection

10 transistors is characterized by an average array pitch equal to the bit line pitch multiplied by an integer other than a power of 2 while they are generally arranged at a pitch equal to the bit line pitch multiplied by a power of 2 (for example, 8 times).

15   The bit line selection transistors are formed in pairs of 2 stages (Q0, Q1), (Q2, Q3), ... (Q14, Q15), each connected to odd and even bit lines adjacent in the bit line direction, sharing a source/drain diffusion layer. In the bit line selection transistors, a channel width W

20 direction (or gate width direction) is laid out to correspond to a direction perpendicular to the bit line. For the bit line selection transistors arranged in the direction perpendicular to the bit line, their gates are formed as common gate lines 11o, 11e to receive the odd and

25 even bit line selection signals DLSo, DLSe.

In the bit line selection transistors, the array pitch b in the gate width W direction (or gate line

direction) may be determined as b - 10a. For the bit line
selection transistors in 10 stages × 8 rows, 16 transistors
are required for every 16 bit lines. As shown, the bit
line selection transistors are arranged in 5 blocks of 16

5   transistors, B0-B4, within a range of 80 bit lines. A
sense amp row 12 comprises sense amp groups S/A<0> - S/A<4>
arranged respectively corresponding to the blocks B0-B4.
Each sense amp group includes 8 sense amps. Connected to
each sense amp group are 8 sensing bit lines, which are led

10   out of the common source/drain diffusion layers in 16 bit
line selection transistors Q0-Q15.

In the example shown in Fig. 1, the total number of
the bit lines is equal to an integer multiple of 80, which
is the least common multiple associated with 16 and 10. In

15   this case, the bit line selection transistors may be
arranged in 10 stages × 8n rows, as described above. In
addition, the bit line selection transistors may have an
array pitch of b = 10a. If the total number of the bit
lines is not equal to an integer multiple of 80, however,

20   it is generally required to interweave the bit line
selection transistors at portions having the number of the
stages different from 10 stages.

Fig. 2 shows a layout of the bit line selection
transistors, when the total number of the bit lines is

25   equal to 80n + 16, corresponding to Fig. 1. In this case,
80n indicates the number of the bit lines arranged in a
region R1, and 16 in a region R2. As previously described,

within the range for 80n bit lines, the bit line selection transistors can be arranged in 10 stages × 2 rows for every 20 bit lines. As for the remaining 16 bit lines, they may be arranged in 8 stages × 2 rows. In this case, the array

5 pitch b of the bit line selection transistors in the gate width W direction may be constant over the whole but is not required to be constant. For example, the bit line selection transistors may be arranged in the direction perpendicular to the bit line at two or more different

10 array pitches. As shown in Fig. 2, in the region R1 for every 20 bit lines, an average transistor array pitch is represented by $b1 = 10a - \alpha/4n$, and in the region R2 for 16 bit lines, it is represented by $b2 = 8a + \alpha$. The bit line selection transistors have an average array pitch of b,

15 which is represented by (the number of bit lines × a)/the number of transistors. Accordingly, $b = (80n + 16)a/(8n + 2) = 10a - 2a/(4n + 1)$. In a word, the average array pitch of the bit line selection transistors in the direction perpendicular to the bit line is equal to a value deviated

20 from an integer multiple of the bit line pitch a.

Figs. 3-7 more specifically show the layout of the bit line selection transistors in Fig. 2 or Fig. 1, including wiring portions, in the respective blocks B0-B4 for every 16 bit lines of the 80 bit lines. Figs. 3, 4, 5,

25 6 and 7 focus attention on B0, B1, B2, B3 and B4 in Figs. 1 and 2, respectively. These blocks B0-B4 correspond to respective column addresses <0> - <4> to input/output 8-bit

data at one column address. In each block, th

corresponding sense amp group is located. For example, the

sense amp group S/A<0> is located in the block B0. The

sense amp group includes 8 sense amps.

5   As shown in Figs. 3-7, the bit line BLo, BLe is

extended and wired from the cell array region to the region

of the bit line selection transistor to be connected, and

connected to the corresponding source/drain diffusion layer

using a lateral wire 13 shown by the dashed line. The

10   lateral wire 13 is a metal wire in a different layer from

the bit line BLo, BLe. In relation to the group of 8 sense

amps, S/A, the sensing bit lines SBL0-7 are arranged in

parallel with the bit lines BLo, BLe in the cell array.

They are each connected to a common diffusion layer between

15   a pair of transistors via a lateral wire shown by the

dashed line. ·

In the example shown in Fig. 2, the total number of

the bit lines is equal to 80n + 16. Alternatively, the

total number of the bit lines may be equal to 80n + 32, 80n

20   + 48, or 80n + 64, for example. In these cases, it is also

required to interweave the bit line selection transistors

at portions having the number of the stages different from

10 stages. In an example shown in Fig. 8, the total number

of the bit lines is equal to 80n + 48. In this case, 80n

25   indicates the number of the bit lines arranged in a region

R3, and 48 in a region R4. As for the section of the 80n

bit lines, except for a delicate deviation in the pitch of

the bit line section from that of the transistor section, the bit line selection transistors may b arranged in 10 stages × 8n rows as explained in Fig. 1. As for the section of the remaining 48 bit lines, the transistors may

5   be arranged in 10 stages × 4 rows + one row of 8 stages as shown in Fig. 8. In this case, the array pitch b of the bit line selection transistors in the gate width direction is represented by b = (80n + 48)a/(8n + 5) = 10a - 2a/(8n + 5) on average.

10   Similarly, if the total number of the bit lines is equal to 80n + 32, not shown, the transistors are arranged in 10 stages × 8n rows + 8 stages × 4 rows. In this case, the array pitch b of the bit line selection transistors in the gate width direction is represented by b = 10a - 2a/(2n

15   + 1) on average. If the total number of the bit lines is equal to 80n + 64, the transistors are arranged in 10 stages × (8n + 4) rows + 8 stages × 3 rows. In this case, the array pitch b of the bit line selection transistors in the gate width direction is represented by b = 10a - 6a/(8n

20   + 7) on average.

In summary, according to this embodiment, the array pitch of the bit line selection transistors in the direction perpendicular to the bit line is more than 8 bit lines and less than 10 bit lines on average. Therefore,

25   this average array pitch of the transistors can be determined to have a value deviated from 10 times or an integer multiple of the bit line pitch. In this case, even

if the bit line selection transistors can not be contained within a period of 8 bit lines, th y can be arranged with margins. In addition, any useless area is not required as is in the arrangement in a period of 16 bit lines. A

5 higher chip area efficiency can be expected while the transistor arrangement is forced to partially differ in number of stages.

In the preceding embodiments, the pair of the bit line selection transistors connected to the adjacent odd

10 and even bit lines BLo, BLe are laid out to align parallel with the bit line direction. To the contrary, if the transistors are rotated by 90°, the pair of the bit line selection transistors connected to the adjacent odd and even bit lines BLo, BLe may be laid out to align parallel

15 with the direction perpendicular to the bit line direction. In other words, the gate length direction intersects the bit line at right angle. A layout of the bit line selection transistors in such an embodiment is shown in Fig. 9.

20 In the example shown in Fig. 9, the width in the gate length direction of the transistor pair can fall within 40 bit lines.

If the total number of the bit lines is equal to an integer multiple of 40, transistor pairs of 20 stages can be

25 arranged within the width of 40 bit lines, bl (= 40a). This is effective to lay out the bit line selection transistors without any useless area. In the example shown

in Fig. 9, however, the total number of the bit lines is represented by a sum of an integer multiple of 40 and an integer multiple of 42. In this case, transistor pairs of 21 stages are arranged within the width of 40 bit lines, b2

5 (= 42a). As a result, the array pitch of the bit line selection transistors in the direction orthogonal to the bit line is determined to have an average larger than b1 and smaller than b2.

The bit lines BLo, BLc and the sensing bit lines SBL

10 can be connected to the corresponding transistor diffusion layers using the lateral intersection wires shown with the dashed lines similar to the preceding embodiments.

Also in this embodiment, the transistor arrangement can be achieved with improved area efficiency while the bit

15 line selection transistors partially differ in number of stages in the bit line direction.

In the examples described in the above embodiments, the sense amps are arranged only at one end of the bit lines. As the bit line pitch is much more finely patterned,

20 the sense amps are often hardly arranged in such the manner. In such the case, it is effective to divide 8 I/Os into two and arrange each 4 I/Os at each of both ends of the bit lines, for example.

As described above, according to the embodiments of

25 the invention, it is possible to provide a semiconductor memory device capable of arranging bit line selection transistors without reduction of the area efficiency.

As an embodiment, an electronic card using the non-volatile semiconductor memory devices according to th above-described embodiments of the present invention and an electronic device using the card will be described bellow.

5   Fig. 10 shows an electronic card according to this embodiment and an arrangement of an electronic device using this card. This electronic device is a digital still camera 101 as an exemplary portable electronic device. The electronic card is a memory card 51 used as a recording

10   medium in the digital still camera 101. The memory card 51 incorporates an IC package PK1 in which the non-volatile semiconductor memory device or the memory system according to the above described embodiments is integrated or encapsulated.

15   The case of the digital still camera 101 accommodates a card slot 102 and a circuit board (not shown) connected to this card slot 102. The memory card 51 is detachably inserted into the card slot 102 of the digital still camera 101. When inserted into the slot 102, the memory card 51 is electrically connected to electric circuits on the

20   circuit board.

If this electronic card is a non-contact type IC card, it is electrically linked to the electric circuits on the circuit board via radio signals when inserted into or

25   approached to the card slot 102.

Fig. 11 shows a basic arrangement of the digital still camera. Light from an object is converged through a

lens 103 and input to an image pickup device 104. The

image pickup d vice 104 is, for exampl , a CMOS sensor and

photoelectrically converts the input light to output, for

example, an analog signal. This analog signal is amplified

5   at an analog amplifier (AMP), and converted into a digital

signal at an A/D converter (A/D). The converted signal is

input to a camera signal processing circuit 105 where the

signal is subjected to automatic exposure control (AE),

automatic white balance control (AWB), color separation,

10   and the like, and converted into a luminance signal and

color difference signals.

To monitor the image, the output signal from the

camera processing circuit 105 is input to a video signal

processing circuit 106 and converted into a video signal.

15   The system of the video signal is, e.g., of the NTSC

(National Television System Committee). The video signal

is input to a display 108 attached to the digital still

camera 101 via a display signal processing circuit 107.

The display 108 is, e.g., a liquid crystal monitor.

20   The video signal is supplied to a video output

terminal 110 via a video driver 109. An image picked up by

the digital still camera 101 can be output to an image

apparatus such as a television set via the video output

terminal 110. This allows the picked-up image to be

25   displayed on an image apparatus other than the display 108.

A microcomputer 111 controls the image pickup device 104,

the analog amplifier (AMP), the A/D converter (A/D), and

the camera signal processing circuit 105.

To capture an image, an operator presses an operation button such as a shutter button 112. In response to this operation, the microcomputer 111 controls a memory

5   controller 113 to write the output signal from the camera signal processing circuit 105 into a video memory 114 as a frame image. The frame image written in the video memory 114 is compressed on the basis of a predetermined compression format by a compressing/ stretching circuit 115.

10   The compressed image is recorded, via a card interface 116, in the memory card 51 inserted into the card slot.

To reproduce a recorded image, an image recorded on the memory card 51 is read out via the card interface 116, stretched by the compressing/stretching circuit 115, and

15   written into the video memory 114. The written image is input to the video signal processing circuit 106 and displayed on the display 108 or another image apparatus in the same manner as the image is monitored.

In this arrangement, those mounted on the circuit

20   board 100 include the card slot 102, the image pickup device 104, the analog amplifier (AMP), the A/D converter (A/D), the camera signal processing circuit 105, the video signal processing circuit 106, the display signal processing circuit 107, the video driver 109, the

25   microcomputer 111, the memory controller 113, the video memory 114, the compressing/ stretching circuit 115, and the card interface 116.

The card slot 102 is not required being mounted on the circuit board 100, and can also be connected to the circuit board 100 via a connector cable or the like.

A power circuit 117 is also mounted on the circuit
5   board 100. The power circuit 117 receives power from an external power source or battery and generates an internal source voltage for use in the digital still camera 101. For example, a DC-DC converter can be used as the power circuit 117. The internal source voltage is supplied to
10   the various circuits described above, in addition to a strobe 118 and the display 108.

As described above, the electronic card according to this embodiment can be used in portable electronic devices such as the digital still camera explained above. However,
15   the electronic card can also be used in various apparatus such as those shown in Figs. 12A to 12J, as well as in portable electronic devices. That is, the electronic card can also be used in a video camera shown in Fig. 12A, a television set shown in Fig. 12B, an audio device shown in
20   Fig. 12C, a game machine shown in Fig. 12D, an electronic musical instrument shown in Fig. 12E, a cell phone shown in Fig. 12F, a personal computer shown in Fig. 12G, a personal digital assistant (PDA) shown in Fig. 12H, a voice recorder shown in Fig. 12I, and a PC card shown in Fig. 12J.
25   The aforementioned embodiments are merely examples and hence do not restrict the present invention. Although a NAND-type flash memory device is explained in the above-

described embodiments, the present invention is applicable to, for example, a NOR-type, a DINOR-type, and the like non-volatile semiconductor memory devices.

While the present invention has been particularly

5 shown and described with reference to the embodiments, it will be understood by those skilled in the art that various changes in form and detail may be made without departing from the spirit, scope, and teachings of the invention.